POKEY-64

POKEY
C012294

BASED

(tmp notes)

CONFIDENTIAL

REVISIONS				DRAWN BY DATE	ATARI INCORPORATED 1265 BORREGAS AVE. [ATARI LOGO] SUNNYVALE, CA. 94086		
M	DESCRIPTION	DATE	APPY'D	CHECKED DATE			
D				ENGINEER	TITLE POKEY CHIP		
				ENGINEERG. MGR.			
				QUALITY ASSURANCE	SIZE A	DRAWING NO. C012294	REV B
				MFG. ENGINEERG.	SCALE	SHEET 1 OF 64	

TABLE OF CONTENTS

TABLE OF ILLUSTRATIONS AND SCHEMAS

1. GENERAL DESCRIPTION

There are thirty two semi-independent audio channels, each with its own frequency, noise and volume control. Each channel has a sixty four bit "divide by N" frequency divider and a sixty four bit control register, which selects the noise (polynomial counter) content and volume.

There are eight key scan lines (K0-K7), which hold a value from 00 to FF. There are two sense lines. One of the sense lines is for the full decode of the eight scan lines. The other sense line is for decoding only the codes (CTRL, SHIFT, BREAK key, and other special keys).

There are eight pot ports for measuring input rise time. Each input has a sixty four bit counter which is clocked every TV line. Each input also has a dump transistor which is turned on or off by software.

There are twenty four timers which use the audio channels. If start timer (STIMER) of selected by STIMER(X) four channels is enabled, the selected four audio channels are reset.

There are eight random number generators which are sixty four bits from a polynomial counters.

There are eight serial I/O ports. Each serial port consists of the serial output lines, the serial input lines, the serial output clock lines, and a bi-directional serial data clock lines. Also there are control registers which are used to configure the serial ports.

There are sixty four IRQ interrupts. They are BREAK key, OTHER key, eight SERIAL INPUT READY, eight SERIAL OUTPUT NEEDED, eight TRANSMISSION FINISHED, twenty four TIMERS and sixteen reserved (see List of IRQ section). These interrupts can be enabled or disabled by software. There are also registers to read interrupts status.

The POKEY-64 system consists of POKEY-64 chip, POKEY-64 Processing Unit (PPU), POKEY-64 Random Access Memory (P-RAM) and POKEY-64 Read Only Memory (P-ROM).

2. AUDIO:

There are thirty two semi-independent audio channels, each with its own frequency, noise, and volume control. Each channel has a sixty four bit "divide by N" frequency divider, controlled by a sixty four bit register (AUDFX). Each channel also has a sixty four bit control register (AUDCX) which selects the noise (polynomial counter) content and the volume.

All thirty two frequency dividers can be clocked simultaneously from 64KHz or 15 KHz by AUDCTL bits on positions 0 of the base 8 bit field format of AUDCTL. Frequency dividers on positions 1 and on positions 3 can alternately be clocked from 1.79 MHz to 1.79 GHz by setting AUDCTL bits on positions 5 and 6. Frequency dividers on positions 2 and 4 can alternately be clocked with the output of dividers on positions 1 and 3 by setting AUDCTL bits on positions 4 and 3. This allows the following options: 32 channels of 64 bit resolution, 16 channels of 128 bit resolution, or 8 channels of 128 bit resolution and 16 channels of 64 resolution, and so on, and 1 channel of 2048 bit resolution.

There are twenty four polynomial counters (eight 136 bit, eight 40 bit and eight 32 bit) used to generate random noise. The 136 bit poly counter can be reduced to a 72 bit poly counter by bits on positions 7 of AUDCTL. These counters are clocked by 1.79 MHz to 1.79 GHz. Their outputs, however, can be sampled independently by the thirty two audio channels at a rate determined by each channel's frequency divider. Thus each channel appears to contain separate poly counters clocked at its own frequency. This poly counter noise sampling is controlled by bits on positions 5, 6, and 7 of each AUDCX register. Because the poly counters are sampled by the "divide by N" frequency divider, the output obviously cannot change faster than the sampling rate. In these modes (poly noise outputted), the dividers are therefore acting as "low pass" filter clocks, allowing only the low frequency noise to pass.

The output of the noise control circuit described above consists of pure tones (square wave type), or polynomial counter noise at a maximum frequency set by the "divide by N" counter (low pass clock). This output can be routed through a high pass filter if desired by use of bits on positions 1 and 2 of AUDCTL.

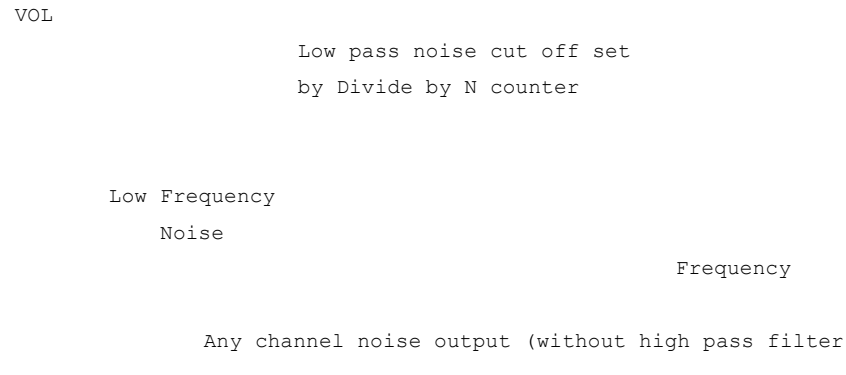
The high pass filter consists of a "D" flip flop and an exclusive-OR Gate. The noise control circuit output is sampled by this flip flop at a rate set by the "High Pass" clock. The input and output of the Flip Flop pass through the exclusive-OR Gate. However, if it is lower than the clock rate, the flip flop output will tend to follow the input and the two exclusive-OR Gate inputs will mostly be identical (11 or 00) giving very little output. This gives the effect of a crude high pass filter, passing noise whose minimum frequency is set by the high pass clock rate. Only channels on positions 1 and 2 have such a high pass filter. The high pass clock for channels on positions 1 comes from the channels on positions 3 divider. The high pass clock for channels on positions 2 comes from the channels on positions 4 divider. This filter is included only if bit on position 1 or 2 of AUDCTL is true.

A volume control circuit is placed at the output of each channel. This is a crude 32 bit digital to analog converter that allows selection of one of 128 possible output current levels for a logic true audio input. A logic zero audio input to this volume circuit always gives an open circuit (zero current) output.

The volume selection is controlled by bits on positions 0 through 3 of AUDCX. "Volume Control only" mode can be invoked by forcing this circuit's audio input true with bits on positions 4 of AUDCX. In this mode the dividers, noise counters, and filter circuits are all disconnected from the channel output. Only the volume control bits (on positions 0 to 3 of AUDCX) determine the channel output current.

The audio output of any channel can be completely turned off by writing zero to the volume control bits of AUDCX. All ones give maximum volume.

AUDIO NOISE FILTERS:



[ATARI LOGO]	TITLE POKEY-64	
	DRAWING NO. REV	SHEET 5 OF 64

AUDCTL (Audio Control) (08, 18, 28, 38, 48, 58, 68, 78): These addresses write data into the Audio Mode Control Register. (Also see SKCTL two-tone bit 3 and notes).

D7-D0 Audio Mode Control Register (AMCR) base field format

D63-D8 (AMCR base field format repeated seven times)	D7	D6	D5	D4	D3	D2	D1	D0

POSITIONS (repeated eight times in one 8-byte AUDCTL, containing independent values which make one full 8-byte AUDCTL, first 8 bits of AUDCTL give standard POKEY AUDCTL):

D7 Change 17 bit poly into a 9 bit below poly
D6 Clock Channel 1 with 1.79 MHz, instead of 64 KHz
D5 Clock Channel 3 with 1.79 MHz, instead of 64 KHz
D4 Clock Channel 2 with Channel 1, instead of 64 KHz (16 bit)
D3 Clock Channel 4 with Channel 3, instead of 64KHz (16 bit)
D2 Insert Hi Pass Filter in Channel 1, clocked by Channel 3 (See section II.)
D1 Insert Hi Pass Filter in Channel 2, clocked by Channel 4
D0 Change Normal 64 KHz frequency, into 15KHz

Positions of bit 7 (D7) in each of repeated base AUDCTL field format:

D63	D55	D47	D39	D31	D23	D15	Base AUDCTL D7

Exact frequencies: The frequencies given above are approximate. The Exact Frequency (Fin) that clocks the divide by N counters is given below (NTSC only, PAL different).

Fin (Approximate)	Fin (Exact)	Use formula for Fout
1.79 MHz	1.78979 MHz	modified
64 KHz	63.9210 KHz	normal
15 KHz	15.6999 KHz	normal

Size of effective poly for one channel consists of eight independently set polys in each of 8 bits on position 7 of AUDCTL base field format.

The Normal Formula for output frequency is:

Fout = Fin/2N

Where N = the binary number in the frequency register (AUDF), plus 1 (N=AUDF+1).

The MODIFIED FORMULA should be used when Fin >= 1.79 MHz and more exact result is desired:

Fout = Fin/2(AUDF + M)

Where: M = 4 if 8 bit counter (AUDCTL bit 3 or 4 = 0)
M = 7 if 16 bit counter (AUDCTL bit 3 or 4 = 1)
[other M values determined in bits on equivalently repeated positions of 64 bit AUDCTL]

AUDF1, AUDF2, AUDF3, AUDF4, AUDF5 to AUDF32 (Audio Frequency) (00, 02, 04, 06, 10 to 76 in format):

These addresses write data into each of the thirty two Audio Frequency Registers. Each register controls a divide by "N" counter.

D7-D0 Audio Frequency Register (AFR) base field format

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0	"N"
	0	0	0	0	0	0	0	0	1
	0	0	0	0	0	0	0	1	2
				ETC.					
	1	1	1	1	1	1	1	1	256

Note: "N" is one greater than the binary number in Audio Frequency Register AUDF(X).

D63-D8 repeated seven times positions D7-D0 of AUDF base field format which make one full 64 bit AUDF

AUDC1, AUDC2, AUDC3, AUDC4, AUDC5 TO AUDC32 (Audio Channel Control) (dec 01, 03, 05, 07, 11 to 77 in format):

These addresses write data into each of the thirty two Audio Control Registers. Each Register controls the noise content and volume of the corresponding Audio Channel.

D7-D0 Audio Control Register (ACR) base field format

Noise Content or Distortion Volume

HEX	D63-D8 (ACR base field format repeated seven times)	D7	D6	D5	D4	D3	D2	D1	D0	Divisor "N" set by audio frequency register.
0		0	0	0	0					- 17 bit poly – 5 bit poly – N
2		0	0	1	0					- 5 bit poly – N - 2
4		0	1	0	0					- 4 bit poly – 5 bit poly – N
5		0	1	1	0					- 5 bit poly – N - 2
8		1	0	0	0					- 17 bit poly - N
A		1	X	1	0					- Pure Tone – N - 2
C		1	1	0	0					- 4 bit poly - N
1		X	X	X	1					- Force Output (Volume only)
0						0	0	0	0	- Lowest Volume (Off)
8						1	0	0	0	- Half Volume
F						1	1	1	1	- Highest Volume

Bits D63 to D8 as a repeated seven times field format of the base 8 bit Audio Control Register give values effective consisted of eight 8 bit base Audio Control Registers to each of the thirty two channels to get the 32 bit noise content and distortion with 32 bit volume control to each of the thirty two channels.

MUSICAL NOTE TABLE

PITCH VALUES FOR THE MUSICAL NOTES-AUDCTL = 0, AUDC = hex AX

		AUDF		
		HEX	DEC	
HIGH NOTES	C	1D	29	Bits 9 to 63 define values between main pitch values (resolution of main musical gamma increases 8 times or define higher or lower values than for standard musical gamma values).
	B	1F	31	
	A# or Bb	21	33	
	A	23	35	
	G# or Ab	25	37	
	G	28	40	
	F# or Gb	2A	42	
	F	2D	45	
	E	2F	47	
	D# or Eb	32	50	
	D	35	53	
	C# or Db	39	57	
	C	30	60	
	B	40	64	
	A# or Bb	44	68	
	A	48	72	
	G# or Ab	4C	76	
	G	51	81	
	F# or Gb	55	85	
	F	5B	91	
	E	60	96	
	D# or Eb	66	102	
	D	6C	108	
	C# or Db	72	114	
MIDDLE C	C	79	121	
	B	80	128	
	A# or Bb	88	136	
	A	90	144	
	G# or Ab	99	153	
	G	A2	162	
	F# or Gb	AD	173	
	F	B6	182	
	E	C1	193	
	D# pr Eb	CC	204	
	D	D9	217	
LOW NOTES	C# or Db	E6	230	
	C	F3	243	

3. KEYBOARD SCAN

The K0-K7 lines hold an 8 bit value from 00 to FF. This allows for decoding 256 keys. With external CMOS (4052-64b) chips, a key matrix is formed. The value of the key selected by the key matrix is returned on the KR1 line.

Internal to the POKEY-64 is an 8 bit binary counter, an 8 bit compare latch, and a 64 bit keycode latch. A control state machine does debouncing of the keys.

When the keyboard scanner is enabled by the SKCTL register, the binary counter begins to count, once per line. If the KR1 line goes low, then value of the binary counter is transferred to compare latch. This will be the key code to be debounced. If KR1 goes low before the next time the binary counter equals the compare latch then there are two keys depressed and both are ignored. If the binary counter equals the compare latch and KR1 is high, then the key is bouncing and is ignored, but if KR1 is low then the key is valid and it is transferred to the keycode latch for reading by the PPU. An IRQ is also sent indicating the key is ready. As soon as KR1 is low and the binary counter equals compare latch, the key is still depressed. As soon as KR1 is high, then the key will be checked for debounce. The next time the binary counter equals the compare latch and KR1 is high, then the key is debounced and another key can be looked for. But if KR1 is low, then the key is bouncing and is assumed to be still pressed.

If the debounce is disabled, the POKEY-64 forces the binary counter equal compare latch signal to a logic true value which will disable debounce.

KR2 input is used to decode 3 keys. They are SHIFT, BREAK and CONTROL. They do not get debounced. They are decoded only at:

		K0	K1	K2	K3	K4	K5
BREAK	=	1	1	1	1	0	0
SHIFT	=	1	1	1	1	0	1
CONTROL	=	1	1	1	1	1	1

BCODE (Keyboard Code) (09): This address reads the Keyboard Code, and is usually read in response to a Keyboard Interrupt (IRQ and bits 6 or 7 of IRQST). See IRQEN for information on enabling keyboard interrupts. See SKCTL bits 1 and 0 for key scan and debounce enable.

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

D63-D10 = RESERVED (see section about Multimedia on POKEY-64 Chip)
D9-D8 = determine keys codes above the standard 6 bit POKEY keys codes (both D9 and D8 zero determine standard 6 bit POKEY keys codes)
D7 = Control Key
D6 = Shift Key

4. POT PORTS

There are eight pot input lines. Each line has a dump transistor and an eight bit latch. There is a binary counter that will count to 28466. The counter is reset by strobing POTGO, which also releases the dump transistors. It also starts the binary counter to count once per line. The pot lines now will start to change. When each line reaches a logic one, it will cause the counter value to be latched into its corresponding latch to be read by the PPU. When the counter reaches 28466, the dump transistor is turned back on to pull the pot lines back to ground. The value in the latches will remain until the next POTGO strobe. To operate pot port:

1) S03->SKCTL ; Turn off init.
2) During VBLANK service routine, perform the following instructons:
   A) Read POT0 to POT7 registers
   B) Write to POTGO register (strobe)

There is an ALLPOT register which allows the logic value of each pot line to be read by the PPU. The main use of ALLPOT is in the fast scan mode. This is done by:

1) Place POKEY in fast scan mode. (See SKCTSL)
2) Write to POTG) address.
3) Wait for cycles of computer clock.
4) Now the ALLPOT register can be read.

NOTE: This address (as well as the fast scan mode) is useful only when the charging capacitors on the P0 – P7 PADS are removed, unless the pads are driven by buffer drivers.

POT0 – POT7 (Pot Values) (00 – 07): These addresses read the value (0 to 28466) of 8 pots (paddle controllers) connected to the 8 lines pot port. The paddle controllers are numbered from left to right when facing the console keyboard. Turning the paddle knob clockwise results in decreasing pot values. The values are valid only after 28466 TV Lines following the “POTGO” command described below or after ALLPOT changes.

D7	D6	D5	D4	D3	D2	D1	D0

Each Pot Value (00-28466)

ALLPOT (All Pot Lines Simultaneously) (08): This address reads the present digital value of the eight line pot port.

D7	D6	D5	D4	D3	D2	D1	D0

Pot number:
7 6 5 4 3 2 1 0

0 = Pot register value is valid.
1 = Pot register value is not valid.

8 Pot Line States

POTGO (Start Pot Scan) (0B, 1B, 2B, 3B, 4B, 5B, 6B, 7B)

No Data Bits Used

This write address starts the pot scan sequence. The pot values (POT0 – POT7) should be read first. This write strobe is then used causing the following sequence:

1) Scan Counter cleared to zero.
2) Capacitor dump transistors turned off.
3) Scan Counter begins counting.
4) Counter value captured in each of 8 registers (POT0 – POT7) as each pot line crosses trigger voltage.
5) Counter reaches 28466, capacitor dump transistors turned on.

5. TIMERS

Three of the four base audio channels can be used as timers. Audio channels on positions 1, 2, and 4 are the channels that will cause IRQ interrupts for the timers. If interrupts are enabled, the interrupts will be caused by the audio channel crossing zero. The audio channel divide can be set to their "AUDF" value by strobing STIMER register. By strobing STIMER, the audio outputs are forced to a known state which are logic high for channels on position 1 and 2, and logic low for channels on position 3 and 4.

STIMER (Start TIMER) (09, 19, 29, 39, 49, 59, 69, 79) (hex)

NOT USED

6. RANDOM NUMBER GENERATORS

There is one hundred thirty six bit polynomial counter that the PPU can read sixty four bit of the counter. The polynomial counter can be changed to nine bits by use of AUDCTL. If the POKEY is in the initial state (see SKCTLS), the counter is set to all ones state, therefore, the PPU will read $FF.

RANDOM (Random Number Generator) (0A, 1A, 2A, 3A, 4A, 5A, 6A, 7A): These addresses read the high order sixty four bits of a 136 bit polynomial counter (9 bit for one 8 bit part of the AUDCTL, if bit 7 of 8 bit part of the AUDCTL = 1).

D63	D55	D47	D39	D31	D23	D15	D7

7. SERIAL PORTS

The serial port consists of a serial data output (transmission) line, a serial data input (receiver) line, a serial output clock line, a bi-directional serial data clock line, and other miscellaneous control lines described in the Operating System Manual. Data is transmitted and received as 64 bits of serial data preceded by a logic zero start bit, and succeeded by a logic true stop bit. Input and output clocks are equal to the baud (bit) rate, not 128 times baud rate. Transmitted data changes when the output clock goes true. Received data is sampled when the input clock goes to zero.

Serial Output: The transmission sequence begins when the processor writes 64 bits of parallel data into the serial output register (SEROUT). When any previous data byte transmission is finished the hardware will automatically transfer new data from (SEROUT) to the output shift register, interrupt the processor to indicate an empty (SEROUT) register (ready t be reloaded with the next byte of data), and automatically serially transmit the shift register contents with start-stop bits attached. If the processor responds to the interrupt, and reloads SEROUT before the shift register is completely transmitted, the serial transmission will be smooth and continuous.

Output data is normally transmitted as logic levels (+4V=true, 0V=false). Data can also be transmitted as two tone information. This mode is selected by bit 3 of SKCTL. In this mode audio channel 1 is transmitted in place of logic true, and audio channel 2 in place of logic zero. Channel 2 must be the lower tone of the tone pair.

The processor can force the data output line to zero (or to audio channel 2, if in two tone mode) by setting bit 7 of SKCTL. This is required to force a break (10 zeros) code transmission.

Serial Output Clock: The serial output data always changes when the serial output clock goes true. The clock then returns to zero in the center of the output data bit time.

The baud (bit) rate of the data and clock is determined by audio channel 4 audio channel 2, or by the input clock, depending on the serial mode selected by bits 4, 5, and 6 of SKCTL. (See chart at end of this section.)

Serial Input: The receiving sequence begins when the hardware has received a complete 64 bit serial data word plus start and stop bits. This data is automatically transferred to the 64 bit parallel input register (SERIN), and the processor is interrupted to indicate an input data byte ready to read in SERIN. The processor must respond to this interrupt, and read SERIN, before the next input data word reception is complete, otherwise an input data "over-run" will occur. This over-run will be indicated by bit 5 of SKSTAT (if bit 5 of IRQST is not RESET (true) before next input complete), and means input data has been lost. This bit should be tested whenever SERIN is read. Bit 7 of SKSTAT should also be tested to detect frame errors caused by extra (or missing) data bits.

Direct Serial Input: The serial data input line can be read directly by the microprocessor if desired, ignoring the shift register, by reading bit 4 of SKSTAT.

Bi-directional Clock: This clock line is used to either receive a clock from an external clock source for checking transmitted or received data, or is used to supply a clock to external devices indicating the transmit or reception rate. This clock line direction is determined by the serial mode selected by bits 4, 5, and 6 of SKCTL. (See mode chart at the end of this section.) Transmitted data changes on the rising edge of this clock. Received data is sampled on the trailing edge of this clock.

Asynchronous Serial Input: Unlocked serial data (at an approximately known (+5%) rate) can be received in the asynchronous modes. The receive (input) shift register is clocked by audio channel 4. Channels 3 and 4 should be used together (AUDCTL bit 3 = 1) for increased resolution. In asynchronous modes, channel 3 and 4 are reset by each start bit at the beginning of each serial data byte. This allows the serial data rate to be slightly different from the rate set by channels 3 and 4.

Serial Mode Control: There are 6 useful modes (of the possible 8) controlled by bits 4, 5, and 6 of SKCTL. These are described on the next page.

Note that two tone output (bit 3 of SKCTL) may be used in any of these modes except for the bottom pair. This is because channel 2 is used to set the output transmit rate and is therefore not available for one of the two tones.

Note that the output clock rate is identical to the output data rate.

SKCTL (Serial Port Control) (0F, 1F, 2F, 3F, 4F, 5F, 6F, 7F): These addresses write data into the registers that control the configuration of the serial ports, and also the Fast Pot Scan, Multimedia Parameters and Keyboard Enable.

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

(Bits perform the functions shown below when true.)

D63-D8 described in other section.

D7 Force Break (force serial output to zero (space))*
D6
D5 Serial Port Mode Control (see mode chart on next page).
D4
D3 Two Tone (Serial output transmitted as two tone signal instead of logic true/false).
D2 Fast Pot (Fast Pot Scan. The Pot Scan Counter completes its sequence in two TV line times instead of one frame time. The capacitor dump transistors are completely disabled.)
D1 Enable Key Scan (Enables Keyboard Scanning circuit)
D0-D1 (Both Zero) Initialize (State used for testing and initializing chip)**

*NOTE: When powered on, serial port output may stay low even if this bit is cleared. To get S. P. high (mark), send a byte out (recommend 00 to FF).

**NOTE: There is no original power on state. POKEY has no reset pin.

SKSTAT (Serial Port-Keyboard Status) (OF, 1F, 2F, 3F, 4F, 5F, 6F, 7F): This address reads the status register giving information about the serial port and keyboard.

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

(Bits are normally true and provide the following information when zero.)

D63-D8 described in other section.

D7 = 0 =
D6 = 0 =
D5 = 0 =
D4 = Serial Input PAD SID Pad
D3 = 0 =
D2 = 0 =
D1 = 0 =
D0 = 1 Not Used (Logic True)

SKRES (Reset above Status Register) (0A, 1A, 2A, 3A, 4A, 5A, 6A, 7A): This write addresses resets bits 7, 6, and 5 of the Serial Port-Keyboard Status Registers to 1.

not used

SERIN (Serial Input Data) (0D, 1D, 2D, 3D, 4D, 5D, 6D, 7D): This addresses read the 64 parallel holding registers that are loaded when full 8-bytes of serial input data have been received. This addresses are usually read in response to a serial data in interrupts (IRQ and bit 5 of base IRQST field format). Also see IRQEN.

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

SEROUT (Serial Output Data) (0D, 1D, 2D, 3D, 4D, 5D, 6D, 7D): This addresses write to the 64 parallel holding registers that are transferred to the output serial shifts registers when a full 8-bytes of serial output data have been transmitted. This addresses are usually written in response to a serial data out interrupts (IRQ and bit 4 of base IRQST field format).

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

8. IRQ INTERRUPTS

There are separate IRQ interrupt enable buts for each IRQ interrupt function (bits 0 through 7 of IRQEN). These bits are not initialized by power turn on, and must be initialized by the program before enabling the processor IRQ. The 8 types of IRQ interrupts are:

D7 = BREAK KEY (depression of the break key)
D6 = OTHER KEY (depression of any other key)
D5 = SERIAL INPUT READY (8-Byte of serial data has been received and is ready to be read by the processor in SERIN register).
D4 = SERIAL OUTPUT NEEDED (8-Byte of serial data is being transmitted and SEROUT is ready to be written to again by the processor).
D3 = TRANSMISSION FINISHED (serial data transmission is finished. Output shift register is empty).
D2 = TIMER # 4 (audio divider # 4 has counted down to zero)
D1 = TIMER # 2 (audio divider # 2 has counted down to zero)
D0 = TIMER # 1 (audio divider # 1 has counted down to zero)

These bits are enabled by bits 0 through 7 of IRQEN and identified by status bits 0 through 7 of IRQST.

The IRQEN register, like the NMIEN register, enables interrupts when its bits are 1 (logic true). The IRQST however (unlike the NMIST) has interrupt status bits that are normally logic true, and go to zero to indicate an interrupt request. The IRQST status bits are returned to logic true only by writing a zero into the corresponding IRQEN bit. This will disable the interrupt and simultaneously set the interrupt status bit to one. Bit 3 of IRQST is not a latch and does not get reset by interrupt disable. It is zero when the serial out is empty (out finished) and true when it is not.

IRQST (IRQ Interrupt Status) (0E, 1E, 2E, 3E, 4E, 5E, 6E, 7E): These addresses read the data from the IRQ Interrupt Status Registers.

0 = Interrupt
1 = No Interrupt

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

D63-D8 described in other section.

D7 = 0 Break Key Interrupt
D6 = 0 Other Key Interrupt
D5 = 0 Serial Input Data Ready Interrupt
D4 = 0 Serial Output Data Needed Interrupt
D3 = 0 Serial Output (Byte) Transmission Finished Interrupt *
D2 = 0 Timer 4 Interrupt
D1 = 0 Timer 2 Interrupt
D0 = 0 Timer 1 Interrupt

*NOTE: Used for question of 2 stop bits.

IRQEN (IRQ Interrupt Enable) (0E, 1E, 2E, 3E, 4E, 5E, 6E, 7E): These addresses write data to the ITQ Interrupt Enable bits.

0 = disable, corresponding IRQST bit is set to 1
1 = enable

D63 - D8	D7	D6	D5	D4	D3	D2	D1	D0

D63-D8 described in other section.

D7 = 0 Break Key Interrupt Enable
D6 = 0 Other Key Interrupt Enable
D5 = 0 Serial Input Data Ready Interrupt Enable
D4 = 0 Serial Output Data Needed Interrupt Enable
D3 = 0 Serial Out Transmission Finished Interrupt Enable
D2 = 0 Timer 4 Interrupt Enable
D1 = 0 Timer 2 Interrupt Enable
D0 = 0 Timer 1 Interrupt Enable

POKEY-64 ADDRESS TABLE

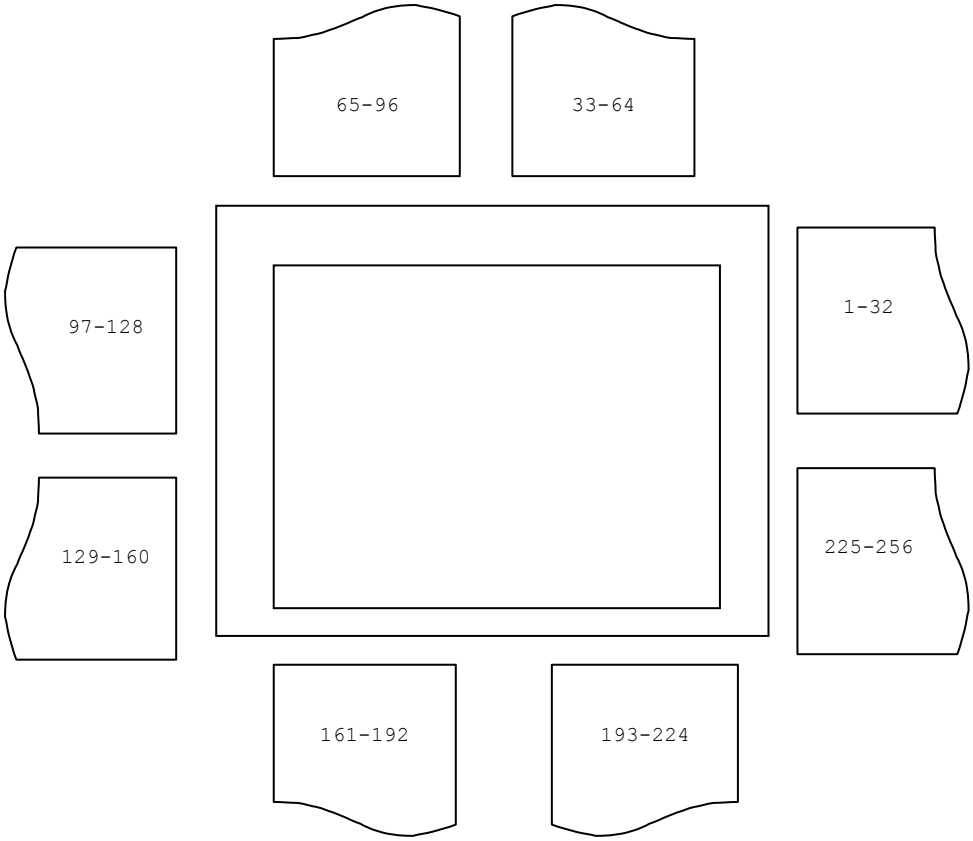
ADDRESS	WRITE		READ	
	Name	Description	Name	Description
0	AUDF1	Audio Channel 1 Frequency	POT0	Read the value of each pot
1	AUDC1	Audio Channel 1 Control	POT1	
2	AUDF2	Audio Channel 2 Frequency	POT2	
3	AUDC2	Audio Channel 2 Control	POT3	
4	AUDF3	Audio Channel 3 Frequency	POT4	
5	AUDC3	Audio Channel 3 Control	POT5	
6	AUDF4	Audio Channel 4 Frequency	POT6	
7	AUDC4	Audio Channel 4 Control	POT7	
8	AUDCTL	Audio Control	ALLPOT	Read 8 line pot port state
9	STIMER	Start timers	KBCODE	Keyboard code
A	SKRES	Reset Status (SKSTAT)	RANDOM	Random number generator
B	POTGO	Start pot scan sequence		
C				
D	SEROUT	Serial port output register	SERIN	Serial port input register
E	IRQEN	IRQ Interrupt enable	IRQST	IRQ Interrupt status register
F	SKCTLS	Serial port 4 key control	SKSTAT	Serial port 4 key status register

[ATARI LOGO]	TITLE POKEY-64	
	DRAWING NO. REV	SHEET 32 OF 64

POKEY-64 PIN LIST

PACKAGE PIN	NAME	FUNCTION	
1	VSS	Ground	I
2	D3	Data Bus	I/O
3	D4	Data Bus	I/O
4	D5	Data Bus	I/O
5	D6	Data Bus	I/O
6	D7	Data Bus	I/O
7	O2	Phase 2 Clock	I
8	P6	Pot Scan	I
9	P7	Pot Scan	I
10	P4	Pot Scan	I
11	P5	Pot Scan	I
12	P2	Pot Scan	I
13	P3	Pot Scan	I
14	P0	Pot Scan	I
15	P1	Pot Scan	I
16	/KR2	Keyboard Scan	I
17	VDD	5 V Power	I
18	/K5	Keyboard Scan	O
19	/K4	Keyboard Scan	O
20	/K3	Keyboard Scan	O
21	/K2	Keyboard Scan	O
22	/K1	Keyboard Scan	O
23	/K0	Keyboard Scan	O
24	SID	Serial Input Data	I
25	/KR1	Keyboard Scan	I
26	BCLK	Bi-direction Clock	I/O
27	OCLK	Serial Output Clock	O
28	SOD	Serial Output Data	O
29	/IRQ	Interrupt Request	O
30	/CSO	Chip Select	I
31	CS1	Chip Select	I
32	R/W	Read/Write Control	I
33	A3	Address Bus	I
34	A2	Address Bus	I
35	A1	Address Bus	I
36	A0	Address Bus	I
37	AUDIO	Audio Out	O
38	D0	Data Bus	I/O
39	D1	Data Bus	I/O
40	D2	Data Bus	I/O
41 to 256	RESERVED		

POKEY-64 BONDING DIAGRAM



SCALE:

PACKAGE:

DIE SIZE:

WIRE BOND:

DIE ATTACH CAVITY:

COMMENT:

Micron Design Rules.

[ATARI LOGO]	TITLE POKEY-64	
	DRAWING NO. REV	SHEET 34 OF 64

POKEY-64 ADDRESS TABLE (EXTENDED)

POKEY-64 Addresses 0 to F repeated 7 times (from 10 (hex) to 7F (hex)):

AUDF5-31	Audio Channels 5 to 31 Frequency
AUDC5-31	Audio Channels 5 to 31 Control
STIMER1-7	Start timers 1 to 7
SKRES1-7	Reset Status (SKSTAT) 1 to 7
SEROUT1-7	Serial port (1 to 7) output registers
SERIN1-7	Serial port (1 to 7) input registers
IRQEN1-7	IRQ Interrupt 1 to 7 enable
IRQST1-7	IRQ Interrupt 1 to 7 status registers
SKCTLS1-7	Serial port (1 to 7) 4 key control
SKSTAT1-7	Serial port (1 to 7) 4 key status registers
RANDOM1-7	Random number generators 1 to 7
POTGO1-7	
POT8-63	
ALLPOT1-7	
KBCODE1-7	for multimedia purposes (see in other section)

[ATARI LOGO]	TITLE POKEY-64	
	DRAWING NO. REV	SHEET -- OF 64

POKEY-64 PIN LIST (RESERVED)

41-68	A4-A31	Address Bus
69-124	D8-D63	Data Bus
125	/K6	Keyboard scan
126	/K7	Keyboard scan
127-133	Audio	Audio Out
135-141	SID	Serial Input Data
142-148	BCLK	Bi-direction Clock
149-155	OCLK	Serial Output Clock
156-162	SOD	Serial Output Data
163-169	R/W	Read/Write Control
170-256		RESERVED for extended POKEY and for Multimedia

Extended POKEY elements:

- 7 times repeated double standard serial I/O port
- added pins for standard serial I/O port to make one double standard serial I/O port
- Serial Input/Output Address Data
- [..]

POLYNOMIAL COUNTERS EFFECTIVE VALUES TABLE (PART OF) - EXAMPLE

List of values effective for eight combined 17 bit or 9 bit poly counters of one 64 bit AUDCTL for one audio channel.

BITS ON POSITION 7 OF BASE AUDCTL FIELD FORMAT								POLY VALUE
D63	D55	D47	D39	D31	D23	D15	D7	
0	0	0	0	0	0	0	0	136
0	0	0	0	0	0	0	1	128
0	0	0	0	0	0	1	0	128
0	0	0	0	0	0	1	1	120
0	0	0	0	0	1	0	0	128
0	0	0	0	0	1	0	1	120
0	0	0	0	0	1	1	0	120
0	0	0	0	0	1	1	1	112
0	0	0	0	1	0	0	0	128
0	0	0	0	1	0	0	1	120
0	0	0	0	1	0	1	0	120
0	0	0	0	1	0	1	1	112
0	0	0	0	1	1	0	0	120
0	0	0	0	1	1	0	1	112
0	0	0	0	1	1	1	0	112
0	0	0	0	1	1	1	1	104
0	0	0	1	0	0	0	0	128
0	0	0	1	0	0	0	1	120
0	0	0	1	0	0	1	0	120
0	0	0	1	0	0	1	1	112
0	0	0	1	0	1	0	0	120
0	0	0	1	0	1	0	1	112
0	0	0	1	0	1	1	0	112
0	0	0	1	0	1	1	1	104
0	0	0	1	1	0	0	0	120
0	0	0	1	1	0	1	0	112
0	0	0	1	1	0	1	1	104
0	0	0	1	1	1	0	0	112
0	0	0	1	1	1	0	1	104
0	0	0	1	1	1	1	0	104
0	0	0	1	1	1	1	1	96

[..]

1	1	1	1	1	1	1	1	72

10. POKEY-64 PROCESSING UNIT

POKEY-64 Processing Unit (PPU) does what was being done by CPU in cooperation with standard POKEY chip.

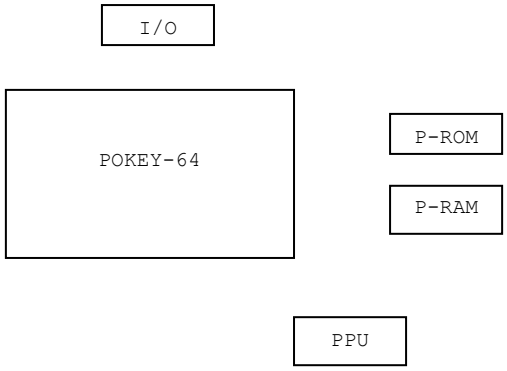
PPU uses in its work own, independent, dedicated POKEY-64 ROM (P-ROM) and own, independent, dedicated POKEY-64 RAM (P-RAM) not interrupting in its work the work of main computer system's CPU (with its own dedicated working independently to POKEY-64 system components).

Main tasks of PPU:

- managing work of POKEY-64 chip
- reading or writing data to/from P-RAM using own data bus and address bus
- reading data from P-ROM using own data bus and address bus
- generating clock cycles
- cooperating with main computer system components through interrupt requests to/from CPU or to/from other components through interrupts or through direct access methods
- executing programs in P-RAM for POKEY-64 system components' desired work (using own set of PPU instructions)

POKEY-64 SYSTEM – GENERAL SCHEMA

IN/OUT THROUGH POKEY-64 STANDARD SOCKET/PORT
IN/OUT THROUGH UNIVERSAL OR DEDICATED SOCKETS OR PORTS



Description:

POKEY-64 system main chips and elements:

PPU – POKEY-64 Processing Unit (managing the POKEY-64 system: main chip, P-RAM, P-ROM, I/O PORTS/SOCKETS, multimedia system)
P-ROM – POKEY-64 Read Only Memory
P-RAM – POKEY-64 Random Access Memory

Main Computer System chips:

RAM – Random Access Memory
CPU – Central Processing Unit

[ATARI LOGO]	TITLE POKEY-64	
	DRAWING NO. REV	SHEET -- OF 64